Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A cache memory system for use in a motion estimation system, comprising:

a first cache memory defined in terms of a first width and a first height, and a second cache memory defined in terms of a second width and a second height, wherein said second height is less than said first height;

the cache memory system being structured in one of two arrangements:

a first arrangement having banks of memory from the second cache memory concatenated vertically such that their concatenated height is at least equal to the first height, and said concatenated banks being arranged to be appended to the width of the first cache memory to form a single contiguous address space, and

a second arrangement having banks of memory from the first and second caches stacked vertically, and arranged to be addressed as two separate address spaces.

2. (Original) A cache memory system as claimed in claim 1 wherein the first and second widths are equal.

3. (Original) A cache memory system as claimed in claim 1 wherein the first arrangement is for use with a motion estimation system having a single search area.

4. (Original) A cache memory system as claimed in claim 1 wherein the second arrangement is for use with a motion estimation system having two separate search areas.

5. (Original) A cache memory system as claimed in claim 4 wherein the two separate search areas are of equal size.

6. (Original) A motion estimation system, comprising a cache memory system that includes:

a first cache memory defined in terms of a first width and a first height, and a second cache memory defined in terms of a second width and a second height, wherein said second height is less than said first height;

the cache memory system being structured in one of two arrangements:

a first arrangement having banks of memory from the second cache memory concatenated vertically such that their concatenated height is at least equal to the first height, and said concatenated banks being arranged to be appended to the width of the first cache memory to form a single contiguous address space, and

a second arrangement having banks of memory from the first and second caches stacked vertically, and arranged to be addressed as two separate address spaces.

7. (Original) A motion estimation system according to claim 6 wherein the motion estimation system is operable according an MPEG standard.

8. (Original) A motion estimation system as claimed in claim 6 wherein the cache memory system is arranged to be addressed as a circular buffer.

9. (Original) A motion estimation system as claimed in claim 6 including means for addressing the cache memory system including:

a start pointer for indicating the start of a search area;

an update pointer for indicating a bank being updated; and

a search width parameter for indicating the extent of the search area.

10. (Original) A method of using a cache memory system in a motion estimation system, the cache memory system including a first cache memory defined in terms of a first width and a first height, and a second cache memory defined in terms of a second width and a second height, wherein said second height is less than said first height, the method comprising:

concatening memory banks of the second cache memory according to one of two arrangements:

concatenating a first one of the memory banks of the second cache vertically on a second one of the memory bank such that the concatenated banks form a single contiguous address space with the first cache memory in a first arrangement, and

concatenating the memory banks of the second memory cache vertically with corresponding memory banks of the first memory cache such that the concatenated banks are arranged to be addressed as two separate address spaces in a second arrangement.

11. (Original) The method of claim 10 wherein the first and second widths are equal.

12. (Original) The method of claim 10, further comprising using the first arrangement as a single logical cache in the motion estimation system by simultaneously searching in the first and second banks of the second cache memory as a single search area.

13. (Original) The method of claim 10, further comprising using the second arrangement as first and second logical caches in the motion estimation system by searching in the memory banks of only the first cache memory as the first logical cache and searching in the memory banks of the second cache memory and in a portion of the memory banks of the first cache memory as the second logical cache.

14. (Original) The method of claim 13 wherein the searching steps are performed simultaneously.

15. (Previously Presented) The method of claim 13 wherein searching in the first logical cache includes searching for forward/backward motion of a video sequence and searching in the second logical cache includes searching for foreground/background motion of the video sequence.

16. (New) A cache memory system as claimed in claim 1 wherein in the second arrangement, each bank of the first cache memory is stacked with a corresponding one of the banks of the second cache memory, thereby forming a set of logical banks that each include one bank of the first cache memory and the corresponding bank of the second cache memory.

17. (New) A cache memory system as claimed in claim 16 wherein in the second arrangement, the two separate address spaces are first and second address spaces, the first address space including first portions of each of the banks of the first cache memory and the second address space including the banks of the second cache memory and second portions of each of the banks of the first cache memory.

18. (New) A motion estimation system according to claim 6 wherein in the second arrangement, each bank of the first cache memory is stacked with a corresponding one of the banks of the second cache memory, thereby forming a set of logical banks that each include one bank of the first cache memory and the corresponding bank of the second cache memory.

19. (New) A motion estimation system according to claim 18 wherein in the second arrangement, the two separate address spaces are first and second address spaces, the first address space including first portions of each of the banks of the first cache memory and the second address space including the banks of the second cache memory and second portions of each of the banks of the first cache memory.

20. (New) A cache memory system for use in a motion estimation system, comprising:

a first cache memory defined in terms of a first width and a first height; and

a second cache memory defined in terms of a second width and a second height, wherein said second height is less than said first height; the second cache memory having banks of memory concatenated vertically such that their concatenated height is at least equal to the first height, and said concatenated banks being arranged to be appended to the width of the first cache memory to form a single contiguous address space.

21. (New) A cache memory system as claimed in claim 20 wherein the first and second widths are equal.

22. (New) A cache memory system for use in a motion estimation system, comprising:

a first cache memory defined in terms of a first width and a first height; and

a second cache memory defined in terms of a second width and a second height, wherein said second height is less than said first height, the second cache memory having banks of memory stacked vertically with respect to corresponding banks of the first cache memory, and arranged to be addressed as two separate address spaces.

23. (New) A cache memory system as claimed in claim 22 wherein the first and second widths are equal.

24. (New) A cache memory system as claimed in claim 22 wherein each bank of the first cache memory is stacked with a corresponding one of the banks of the second cache memory, thereby forming a set of logical banks that each include one bank of the first cache memory and the corresponding bank of the second cache memory.

25. (New) A cache memory system as claimed in claim 24 wherein the two separate address spaces are first and second address spaces, the first address space including first portions of each of the banks of the first cache memory and the second address space including the banks of the second cache memory and second portions of each of the banks of the first cache memory.